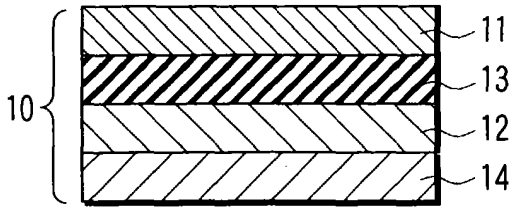
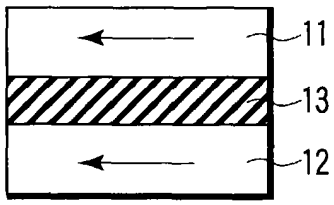
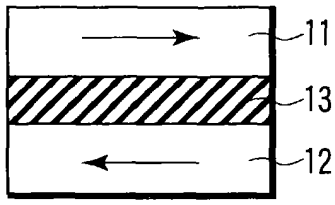


FIG. 1
(PRIOR ART)



Parallel (Low resistance)

FIG. 2A
(PRIOR ART)



Anti-parallel (High resistance)

FIG. 2B
(PRIOR ART)

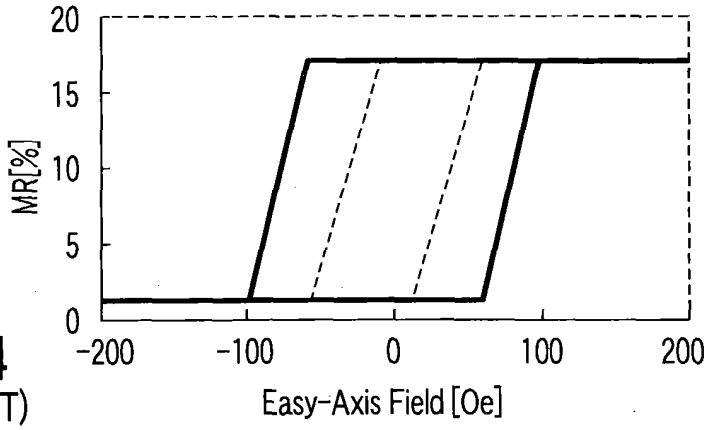


FIG. 4
(PRIOR ART)

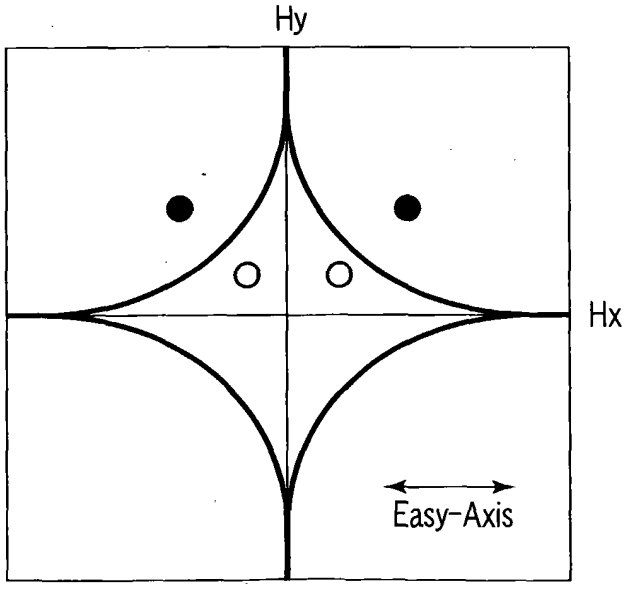


FIG. 5
(PRIOR ART)

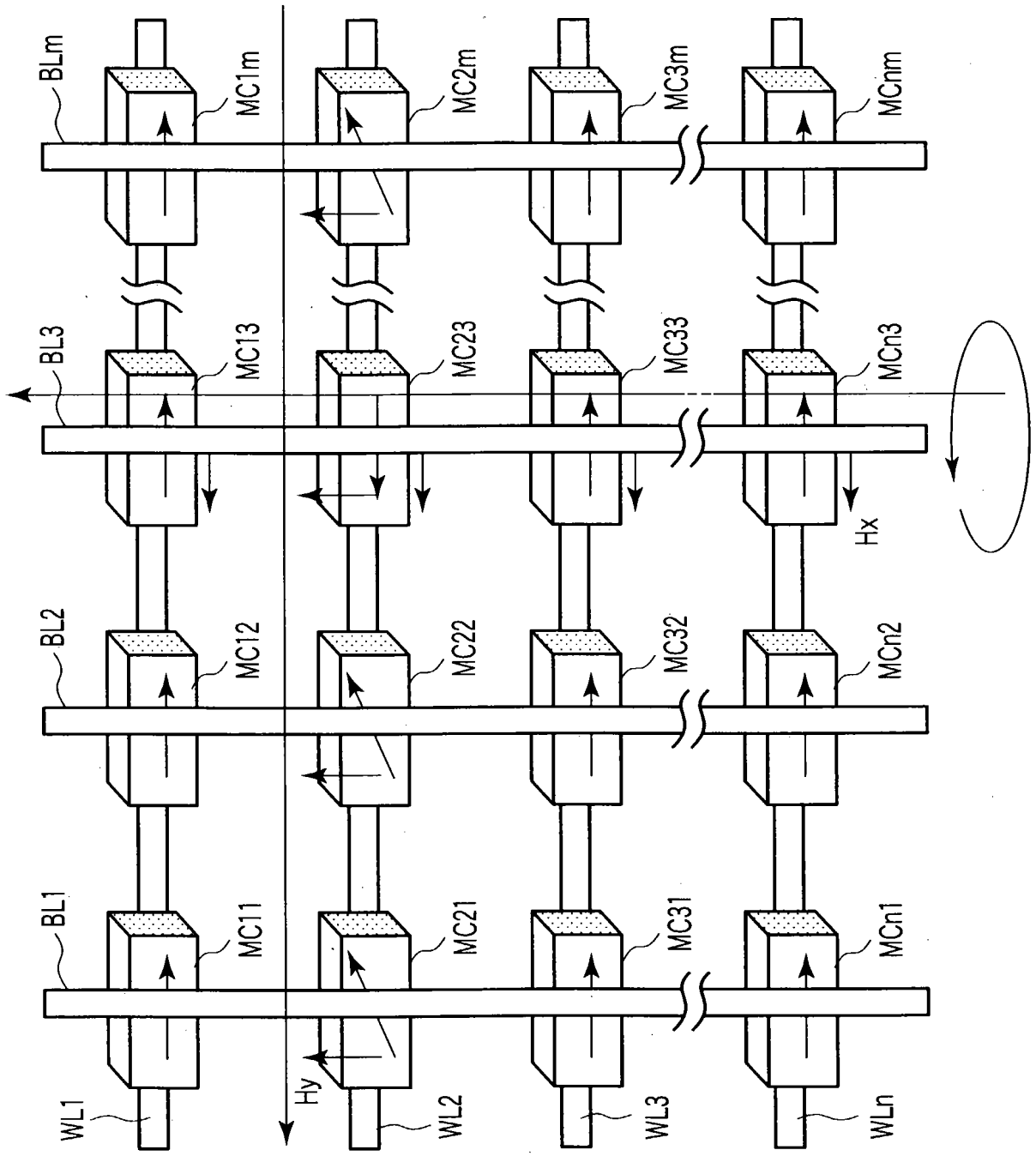


FIG. 3
(PRIOR ART)

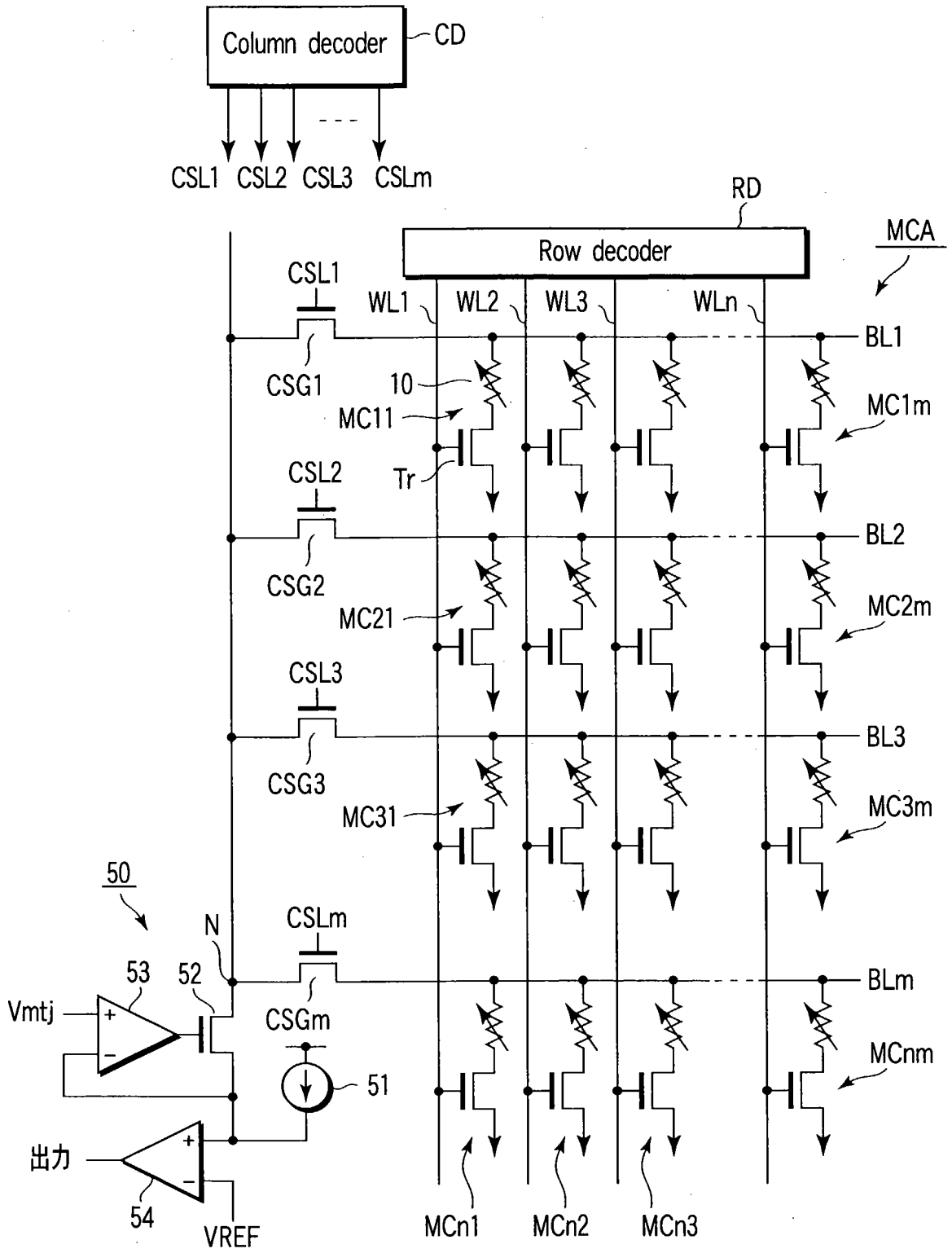

Column decoder
CD
CSL1
CSL2
CSL3
CSLm
RD
Row decoder
MCA
WL1
WL2
WL3
WLn
BL1
BL2
BL3
BLm
CSG1
CSG2
CSG3
CSGm
10
MC11
MC21
MC31
MC1m
MC2m
MC3m
MCnm
Tr
50
N
53
52
Vmtj
51
出力
54
VREF
MCn1
MCn2
MCn3

FIG. 6

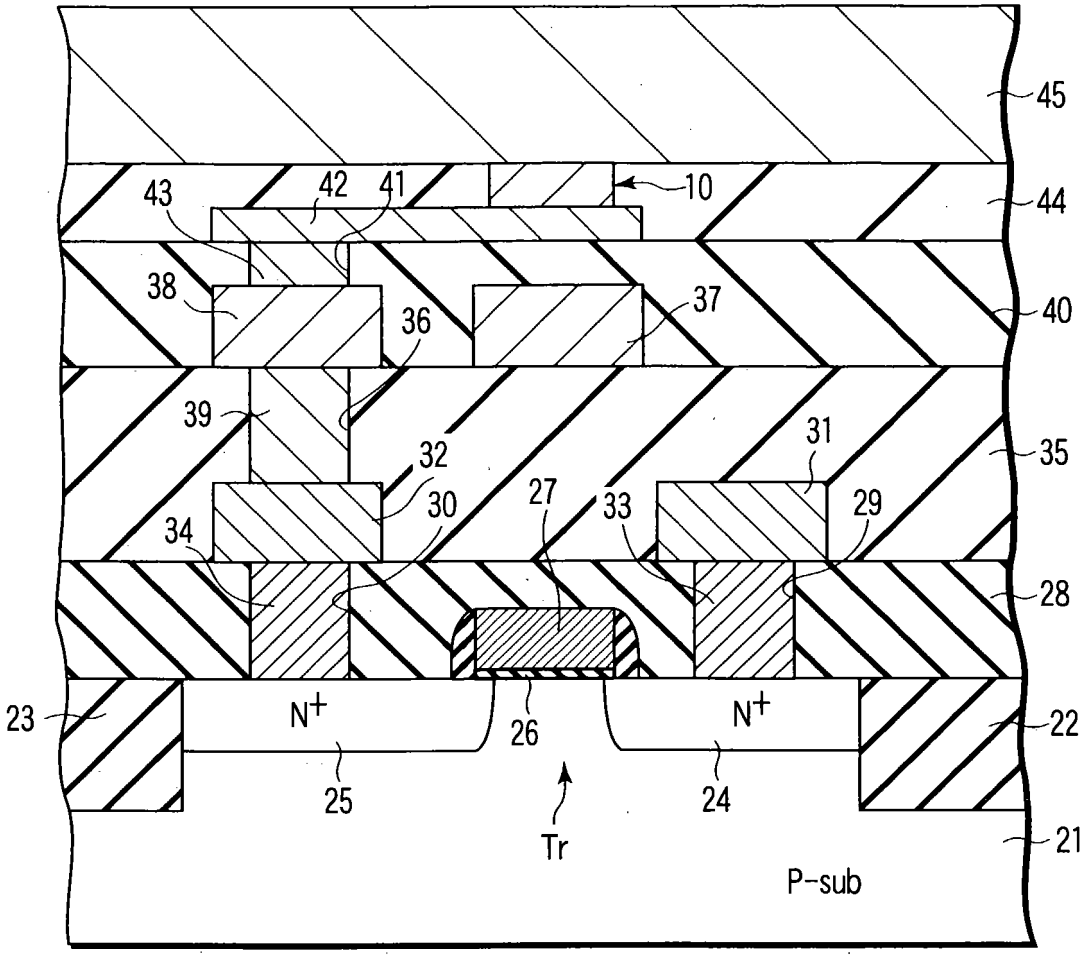

45
44
43
42
41
10
38
36
37
40
39
32
31
35
34
30
27
33
29
28
23
N+
26
N+
22
25
24
Tr
21
P-sub

FIG. 7

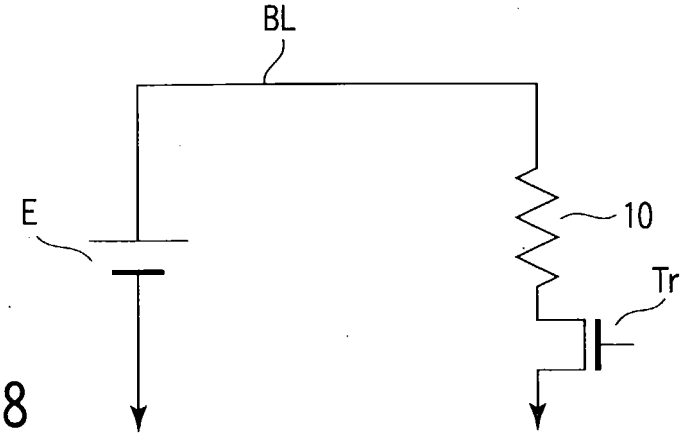

BL
E
10
Tr

FIG. 8

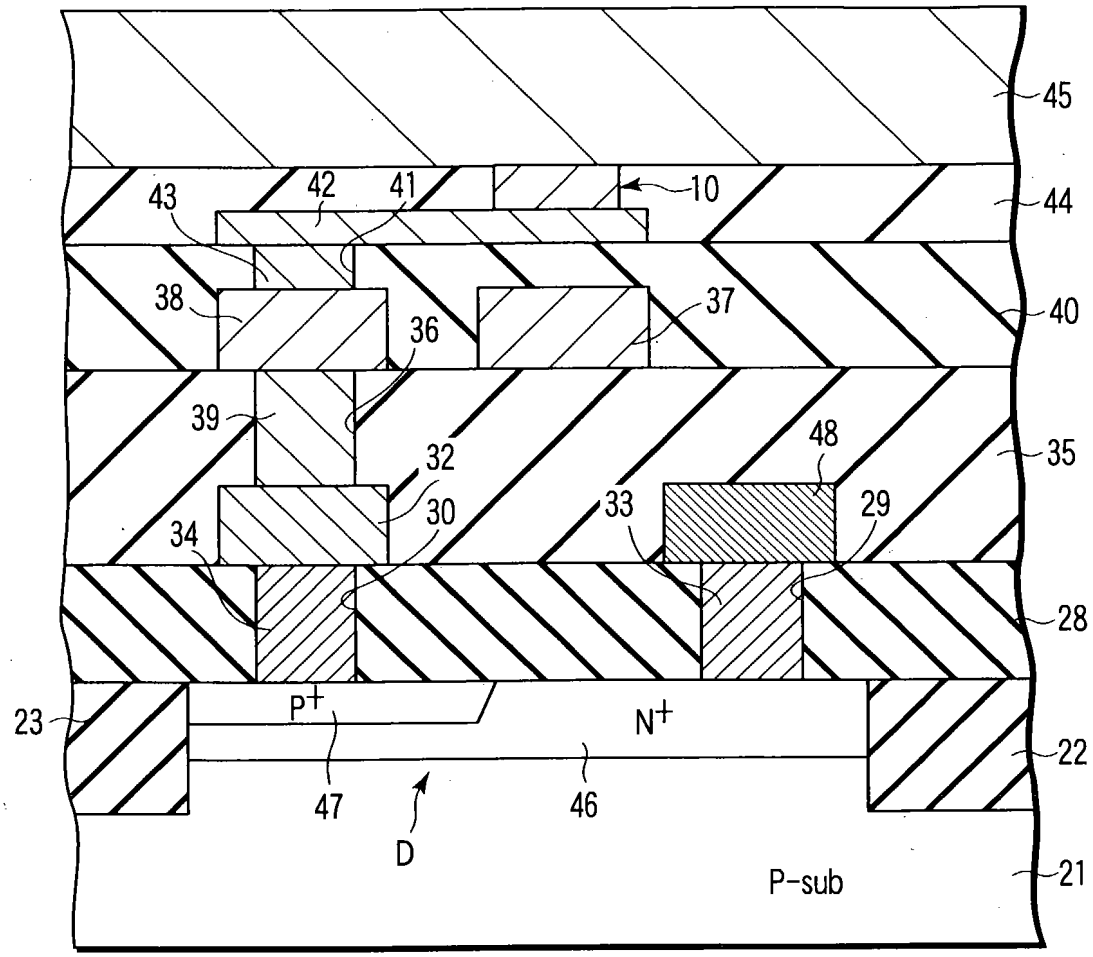

45
44
43
42
41
10
38
37
40
36
39
48
35
32
30
33
29
34
28
23
P+
N+
22
47
46
D
P-sub
21

FIG. 9

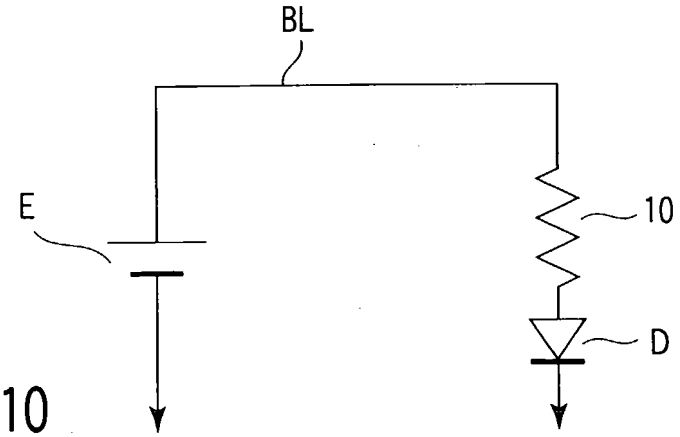

BL
E
10
D

FIG. 10

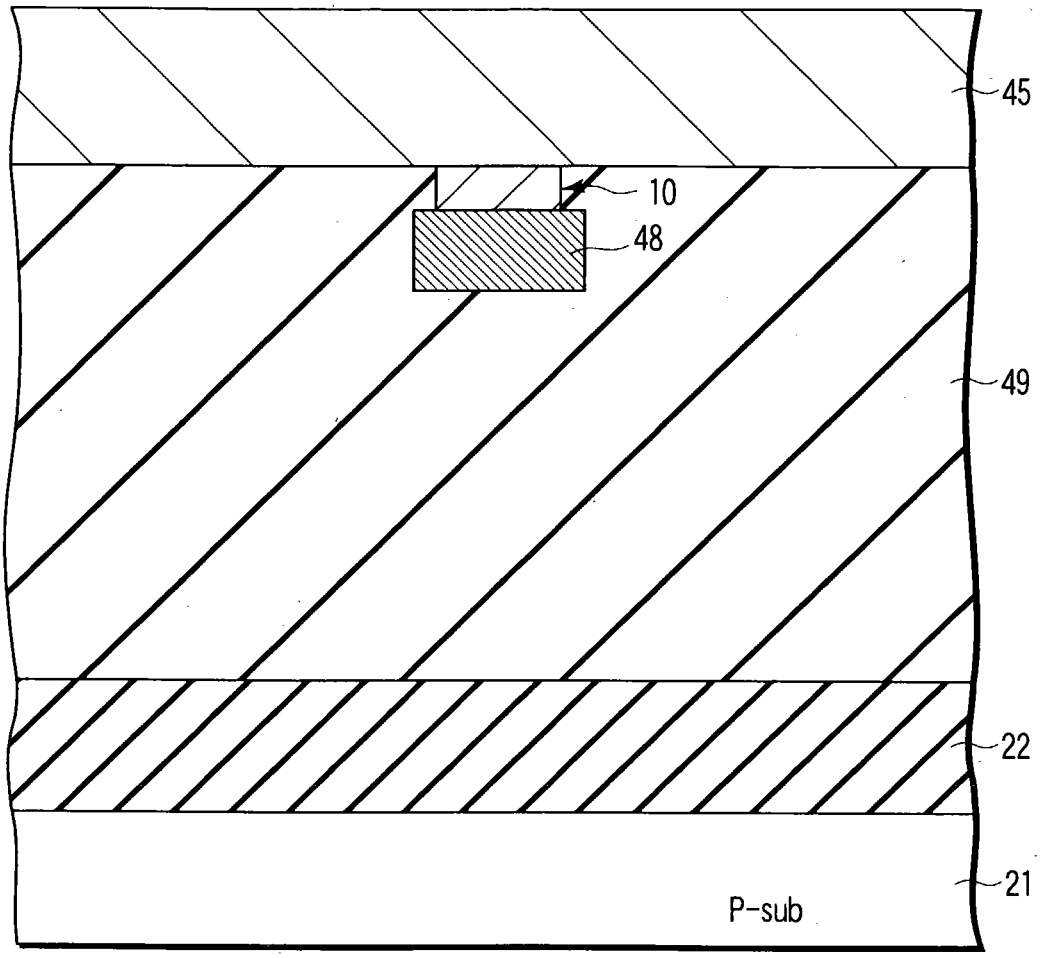


FIG. 11

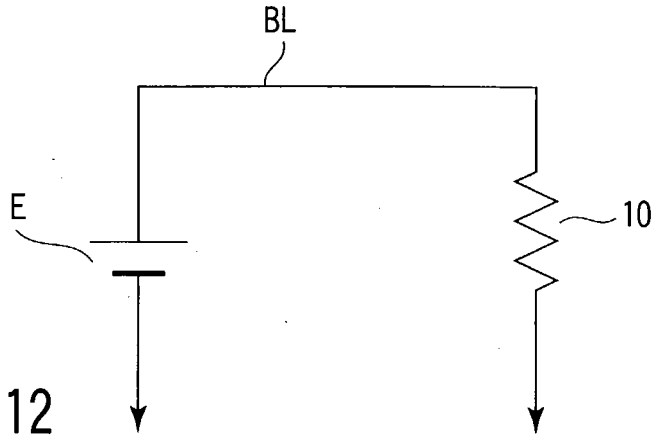


FIG. 12

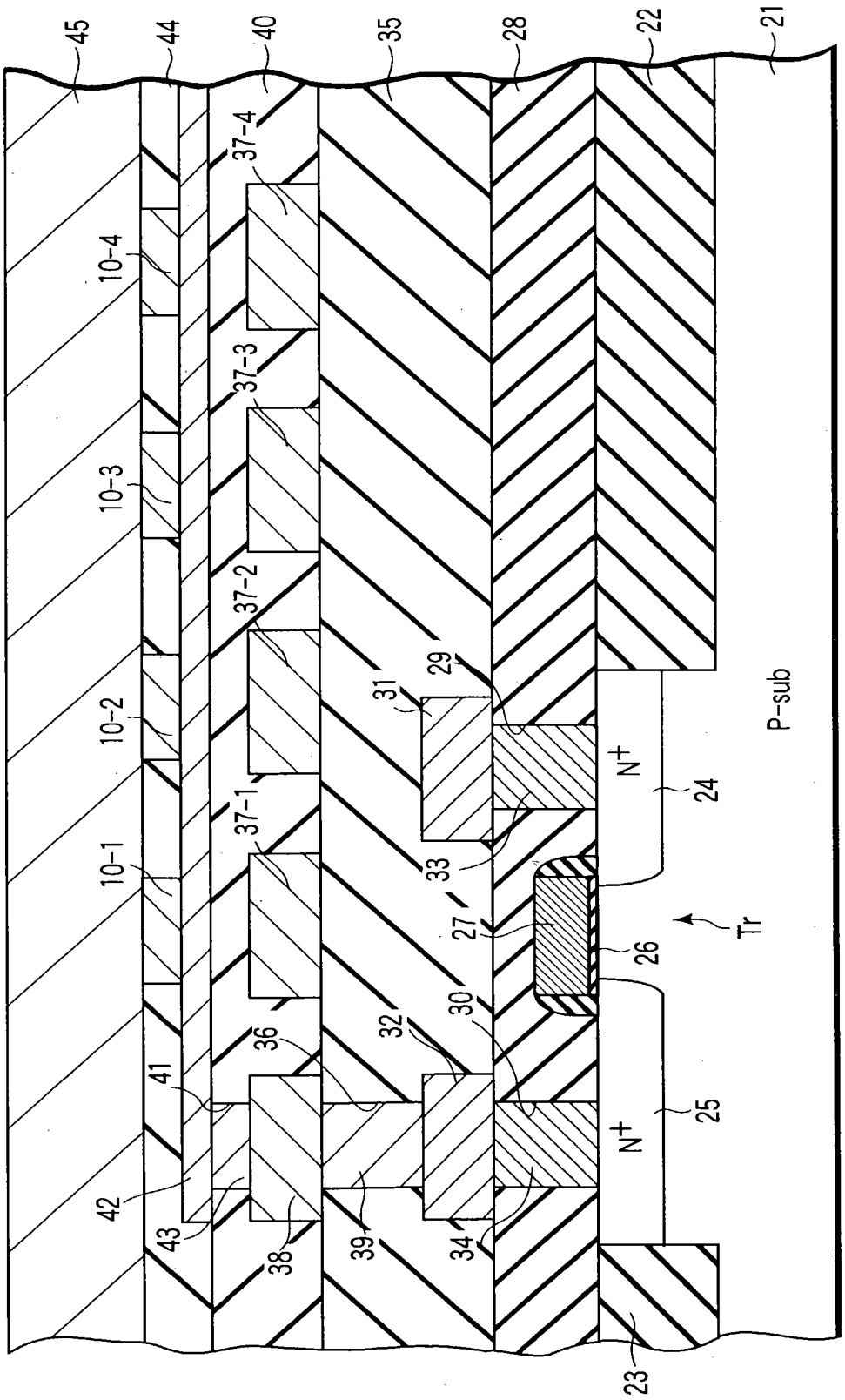

45
44
40
35
28
22
21
37-4
10-4
37-3
10-3
37-2
10-2
37-1
10-1
31
29
33
27
26
30
32
36
41
42
43
38
39
34
N+
24
N+
25
Tr
P-sub
23

FIG. 13A

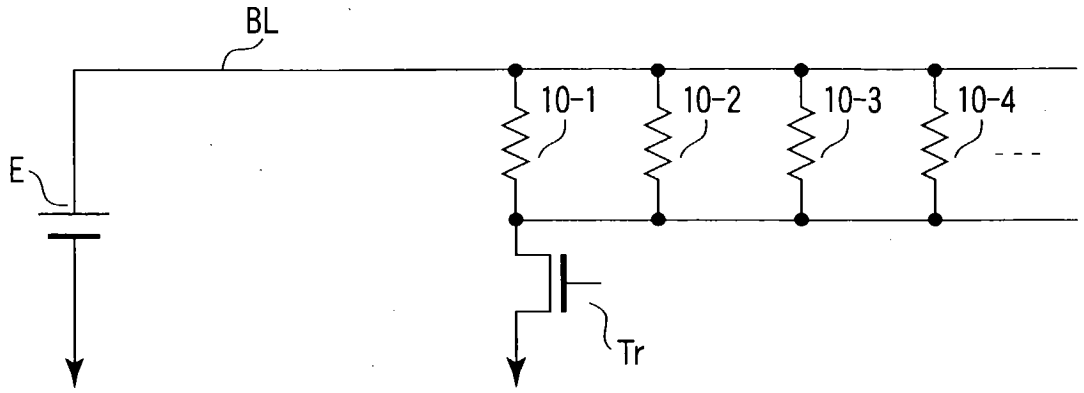


FIG. 13B

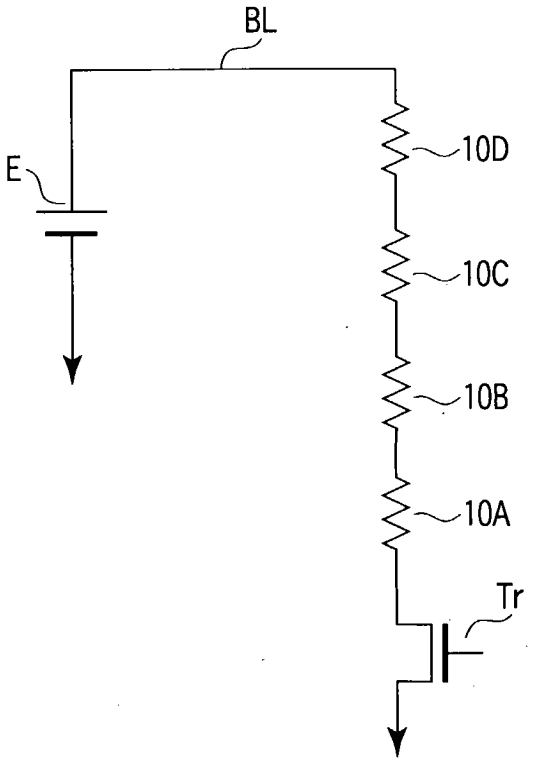


FIG. 14B

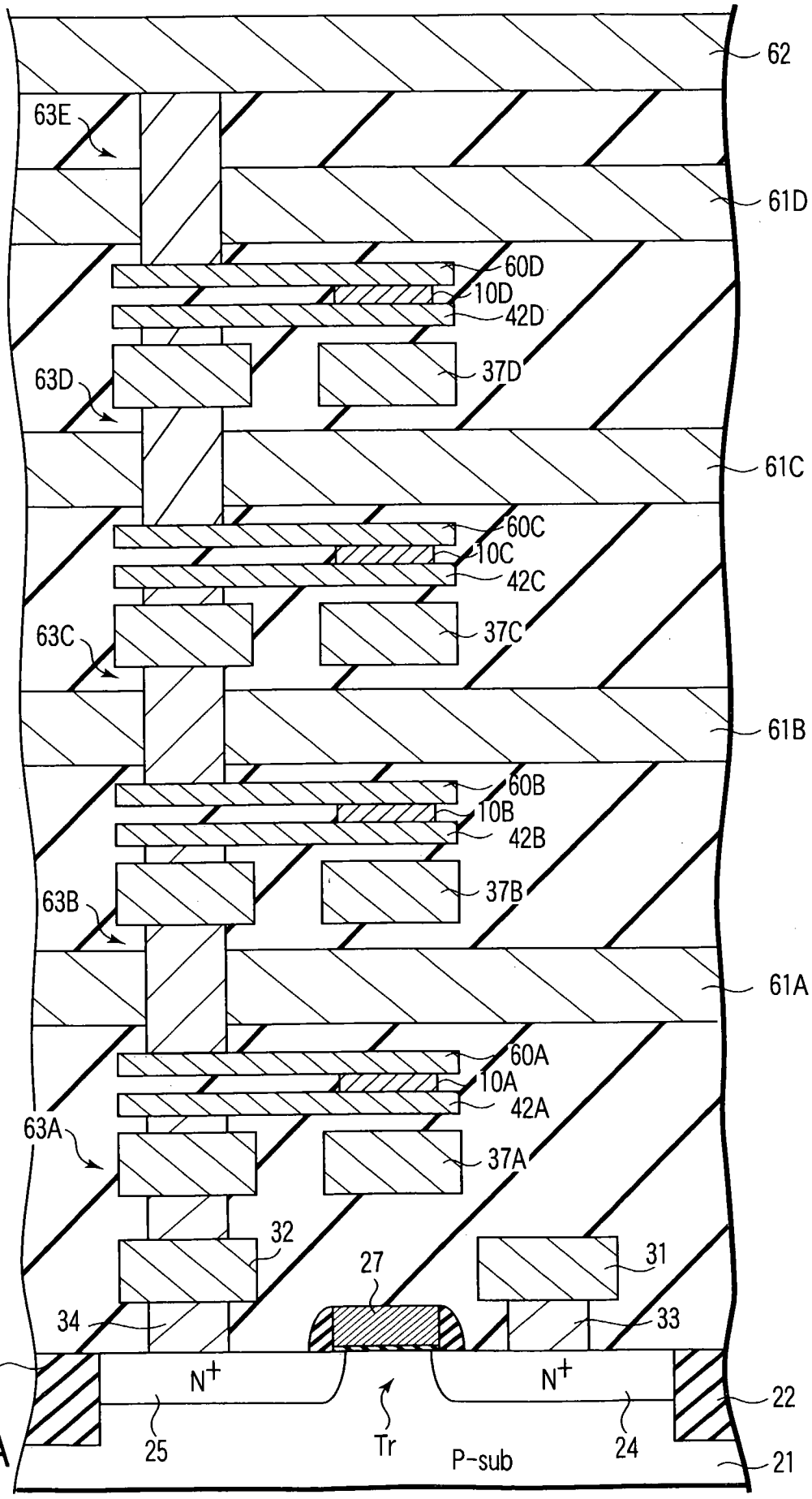

62
63E
61D
60D
10D
42D
37D
63D
61C
60C
10C
42C
37C
63C
61B
60B
10B
42B
37B
63B
61A
60A
10A
42A
37A
63A
32
31
27
34
33
23
N+
N+
22
25
Tr
24
P-sub
21

FIG. 14A

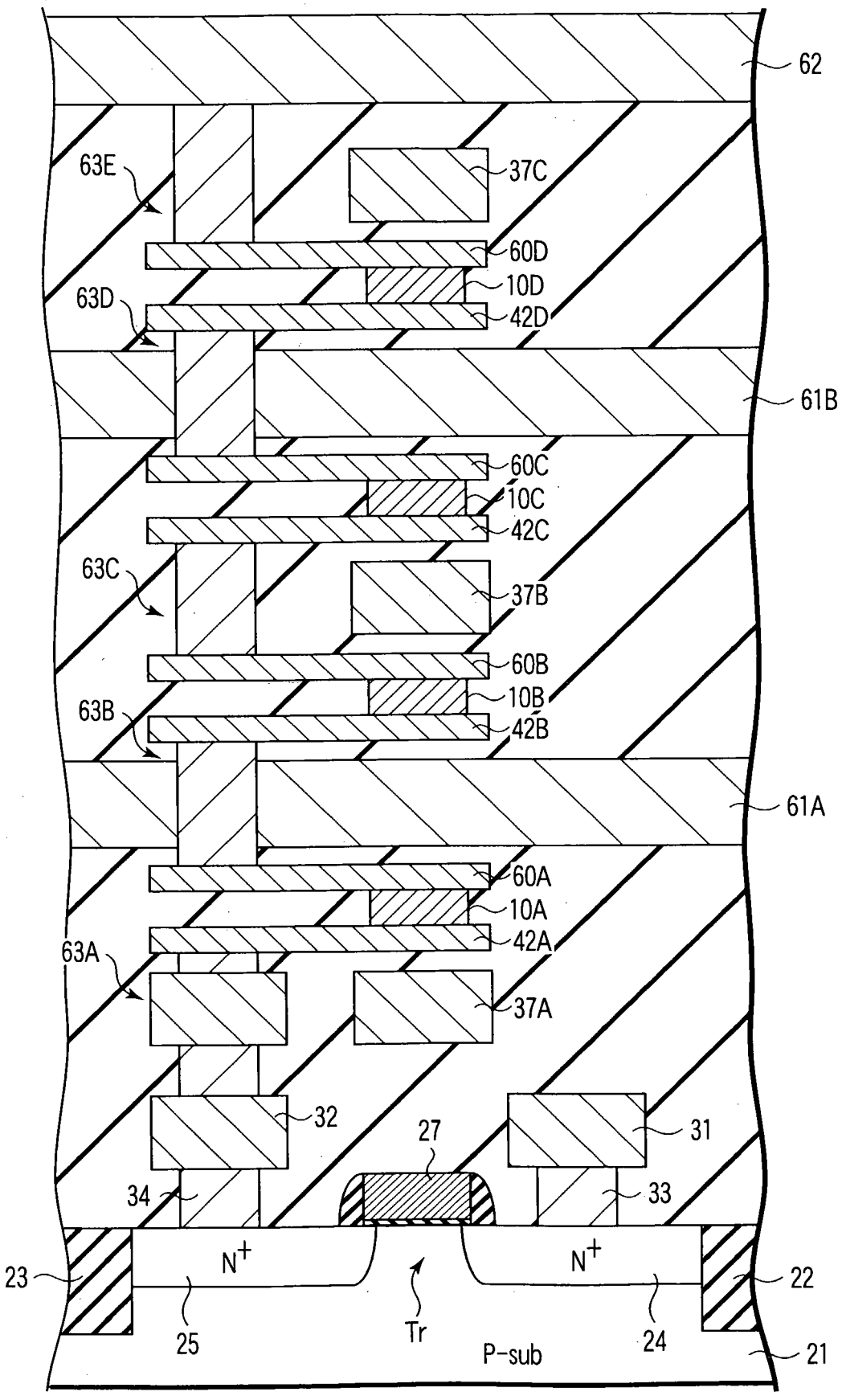

62
63E
37C
60D
10D
63D
42D
61B
60C
10C
42C
63C
37B
60B
10B
63B
42B
61A
60A
10A
42A
63A
37A
32
27
31
34
33
23
N+
N+
22
25
Tr
24
P-sub
21

FIG. 15

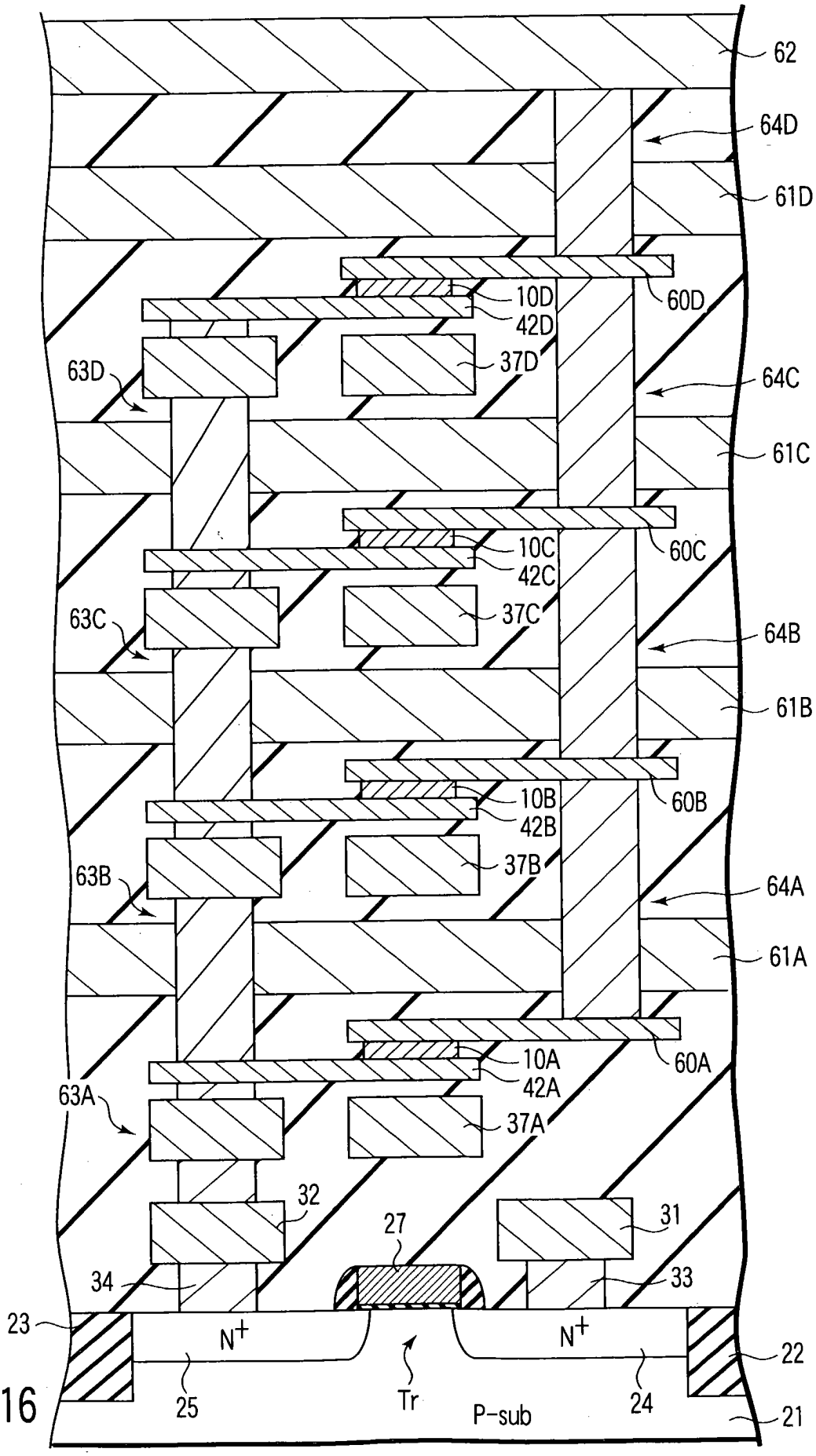

62
64D
61D
10D
42D
60D
37D
63D
64C
61C
10C
42C
60C
37C
63C
64B
61B
10B
42B
60B
37B
63B
64A
61A
10A
42A
60A
37A
63A
32
31
27
34
33
23
N+
N+
22
25
Tr
24
P-sub
21

FIG. 16

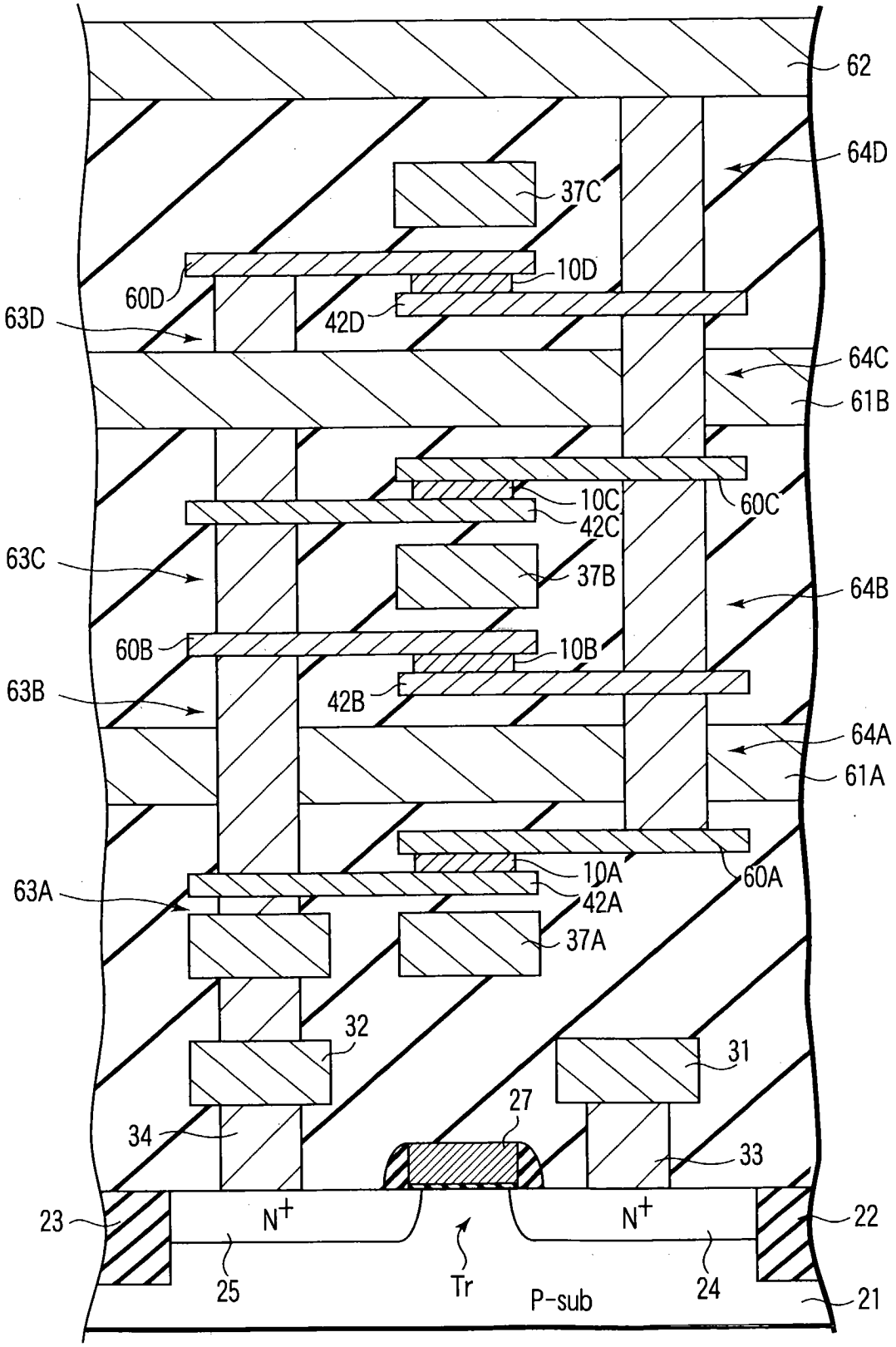

62
64D
37C
10D
60D
63D
42D
64C
61B
10C
42C
60C
63C
37B
64B
60B
10B
63B
42B
64A
61A
10A
60A
63A
42A
37A
32
31
27
34
33
23
N+
N+
22
25
Tr
24
P-sub
21

FIG. 17

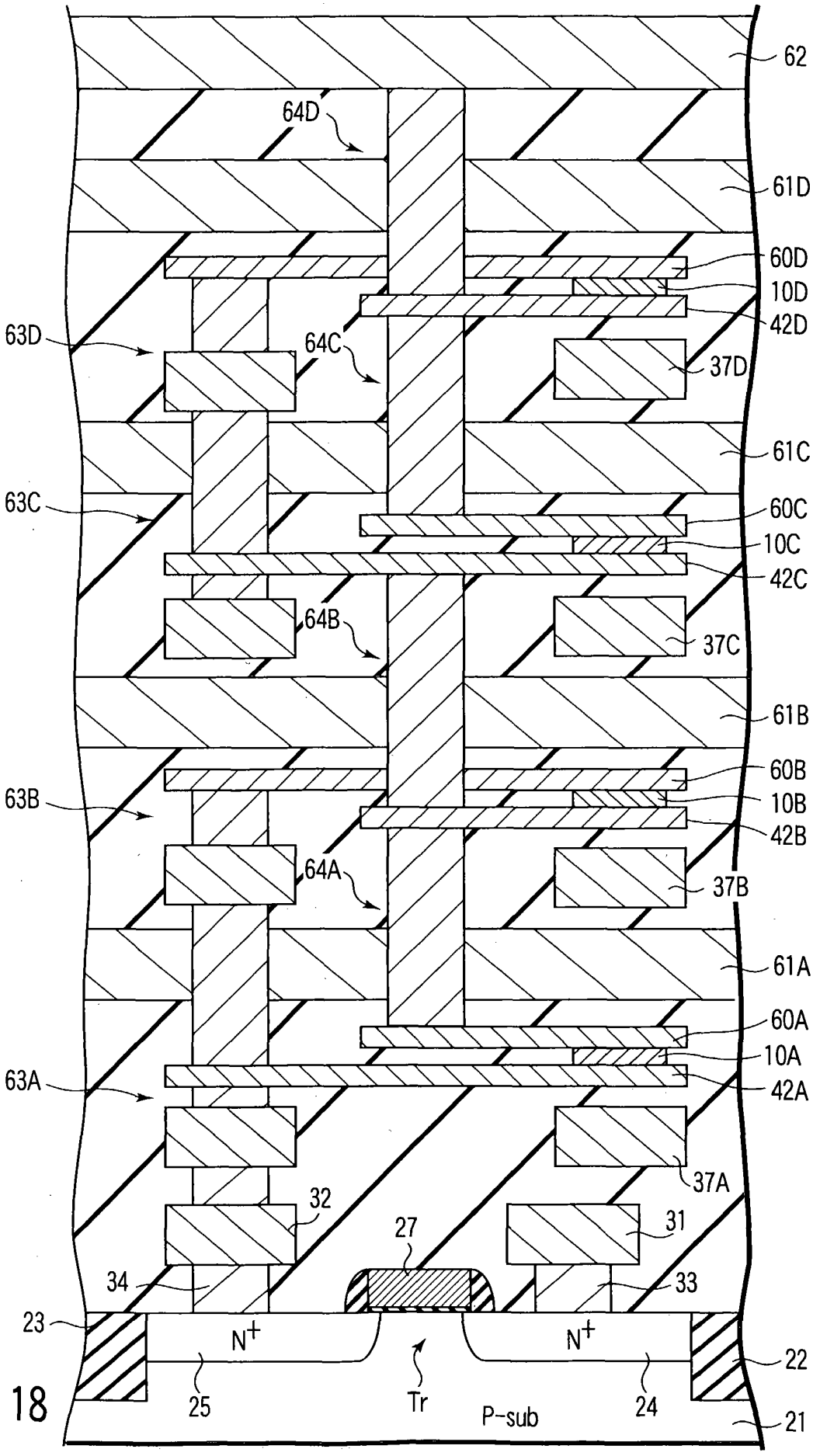

62
64D
61D
60D
10D
42D
63D
64C
37D
61C
63C
60C
10C
42C
64B
37C
61B
60B
63B
10B
42B
64A
37B
61A
60A
10A
63A
42A
37A
32
31
27
34
33
23
N+
N+
22
25
Tr
24
P-sub
21

FIG. 18

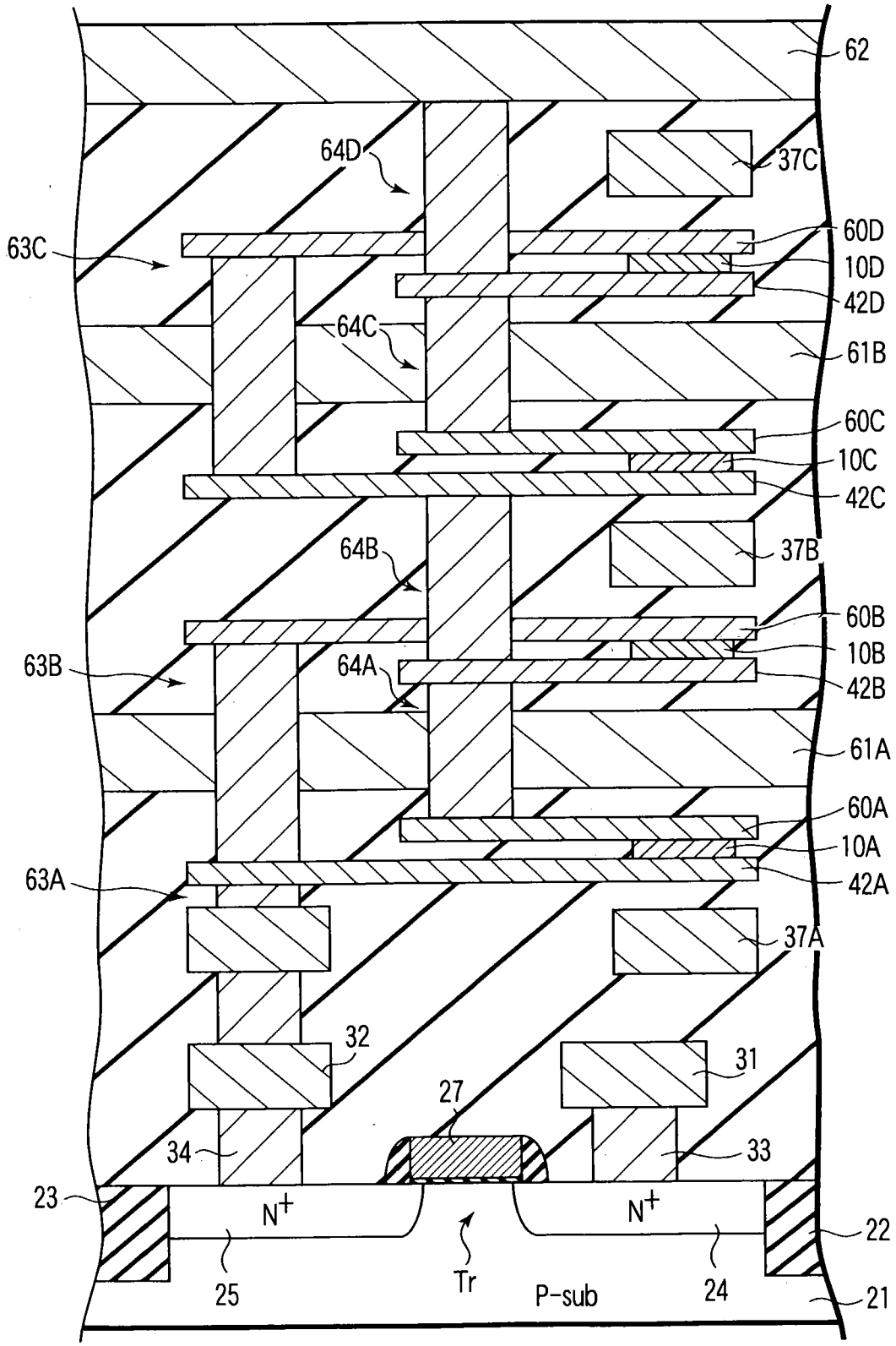

62
64D
37C
63C
60D
10D
42D
64C
61B
60C
10C
42C
64B
37B
60B
63B
10B
64A
42B
61A
60A
10A
63A
42A
37A
32
31
27
34
33
23
N+
N+
22
25
Tr
P-sub
24
21

FIG. 19

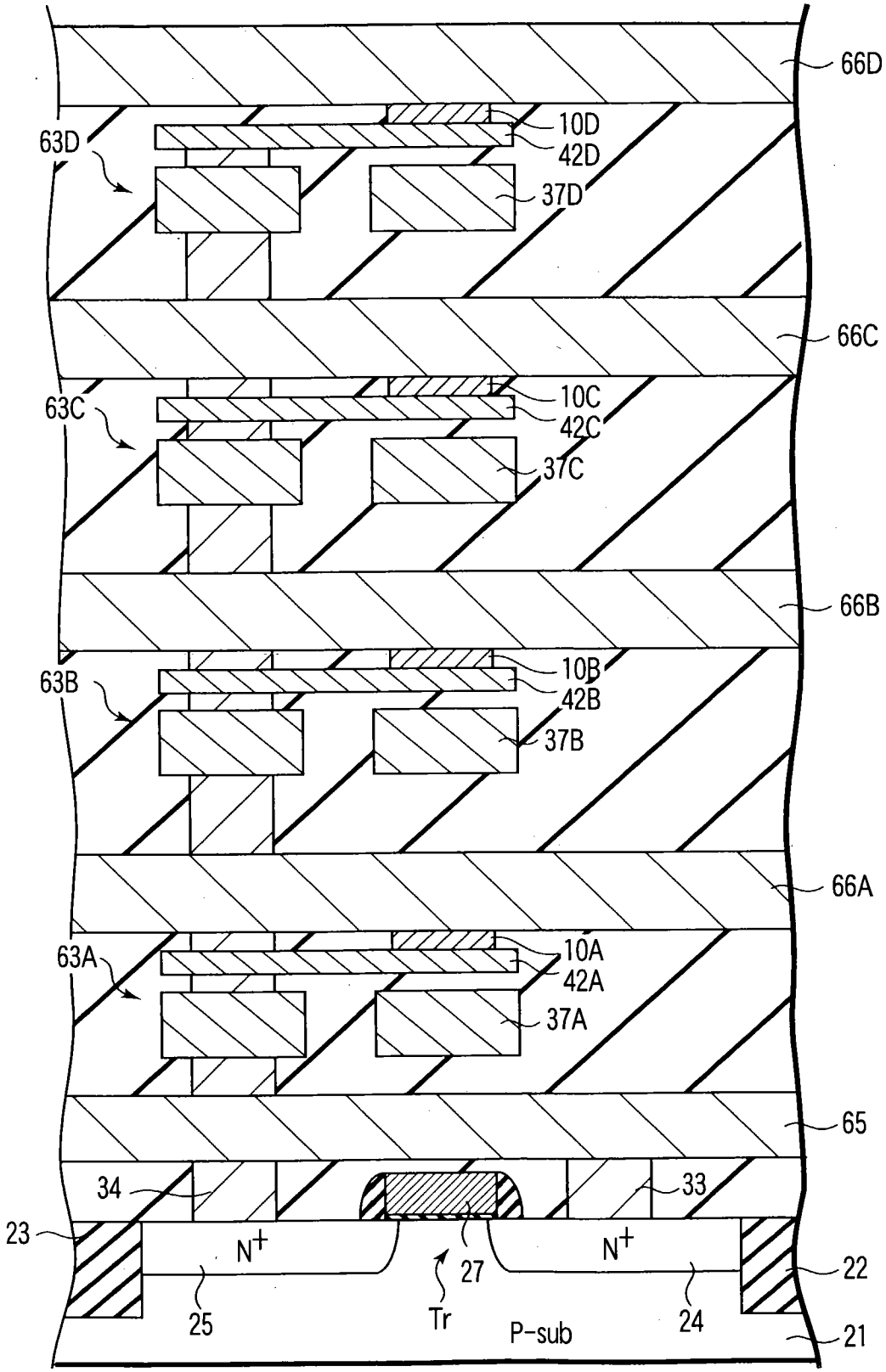

66D
63D
10D
42D
37D
66C
63C
10C
42C
37C
66B
63B
10B
42B
37B
66A
63A
10A
42A
37A
65
34
33
23
N+
N+
22
27
25
Tr
24
P-sub
21

FIG. 20

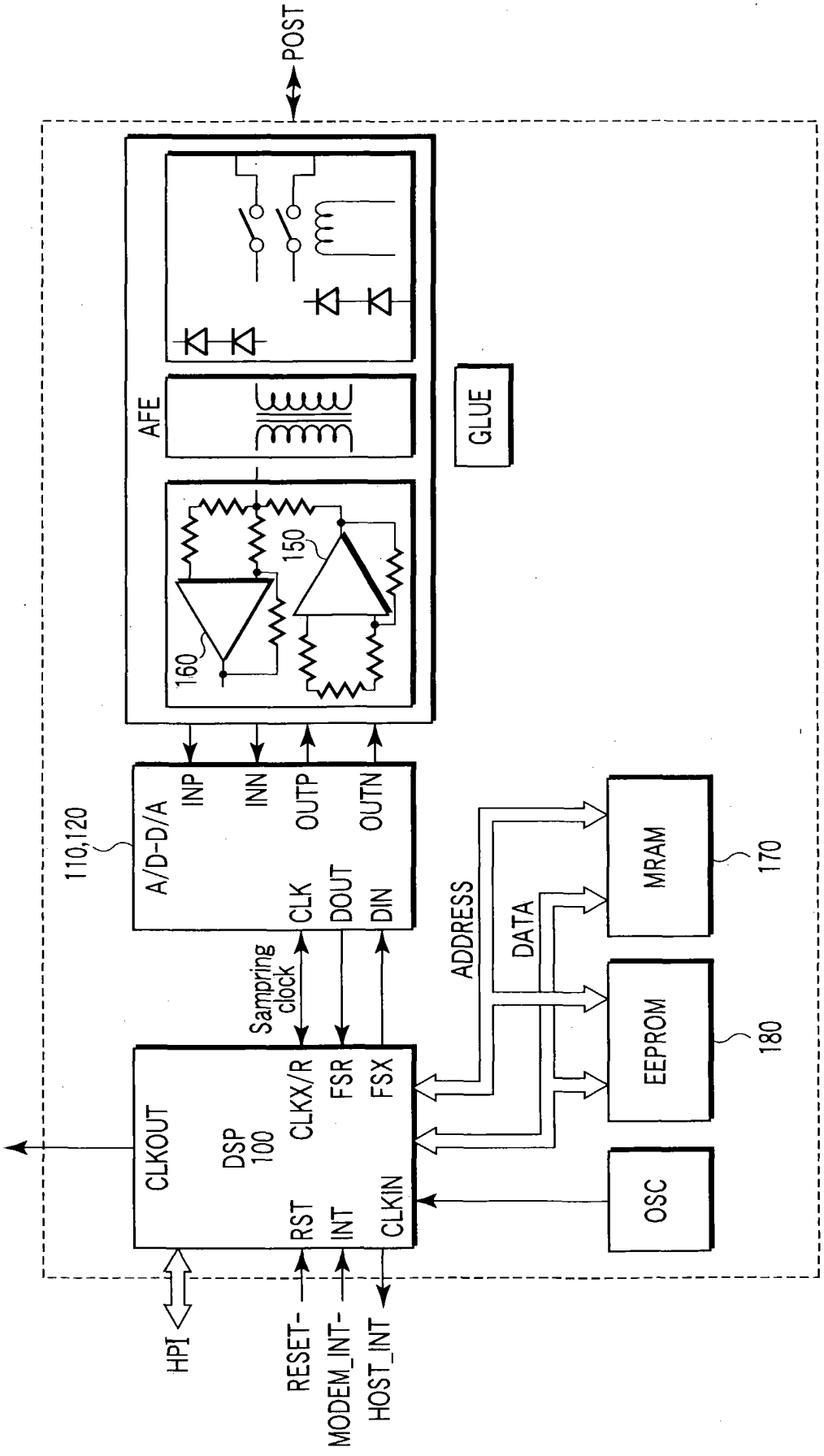

POST
AFE
GLUE
150
160
110,120
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
Sampring clock
ADDRESS
DATA
MRAM
170
EEPROM
180
OSC
CLKOUT
DSP
100
CLKX/R
FSR
FSX
RST
INT
CLKIN
HPI
RESET-
MODEM_INT-
HOST_INT

FIG. 21

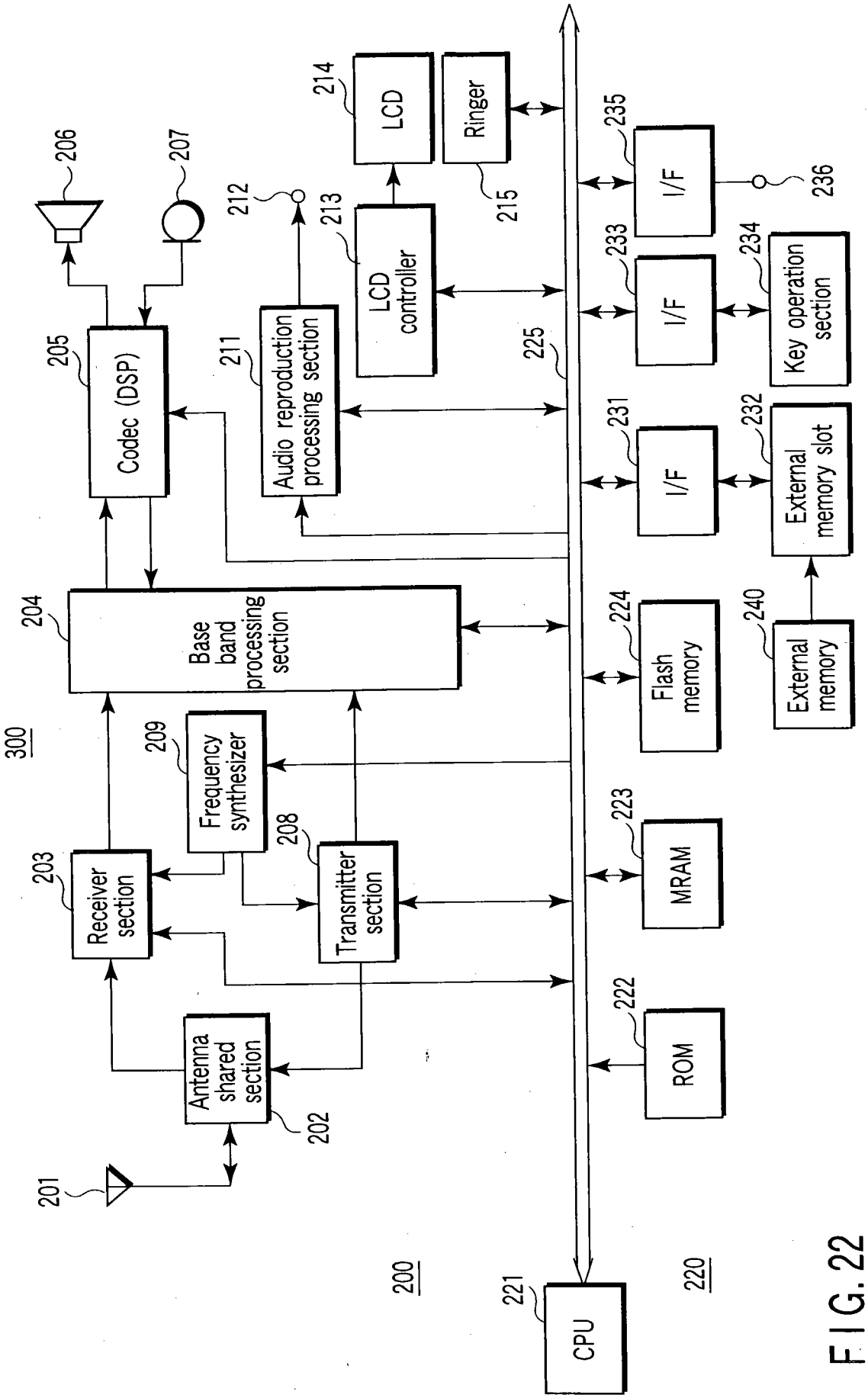

206
207
212
214
LCD
Ringer
235
I/F
236
213
LCD controller
215
233
I/F
234
Key operation section
205
Codec (DSP)
211
Audio reproduction processing section
225
231
I/F
232
External memory slot
204
Base band processing section
224
Flash memory
240
External memory
300
209
Frequency synthesizer
208
203
Receiver section
Transmitter section
223
MRAM
222
ROM
Antenna shared section
202
201
200
221
CPU
220

FIG. 22

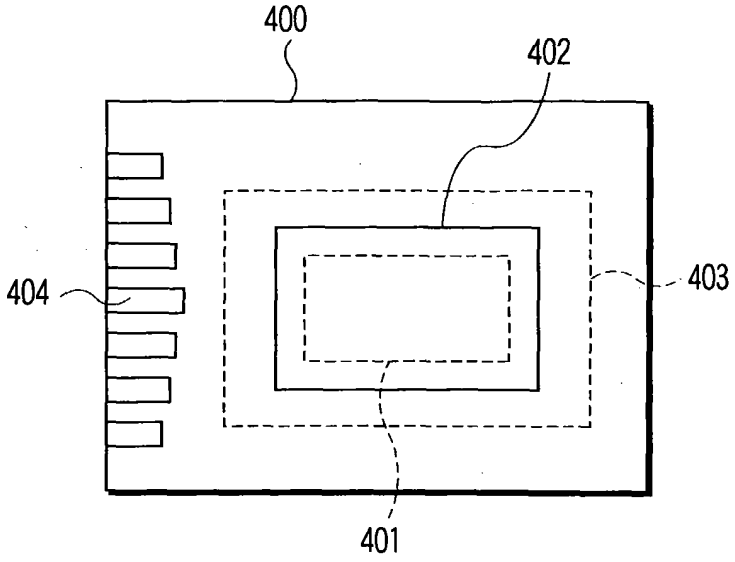

400
402
404
403
401

FIG. 23

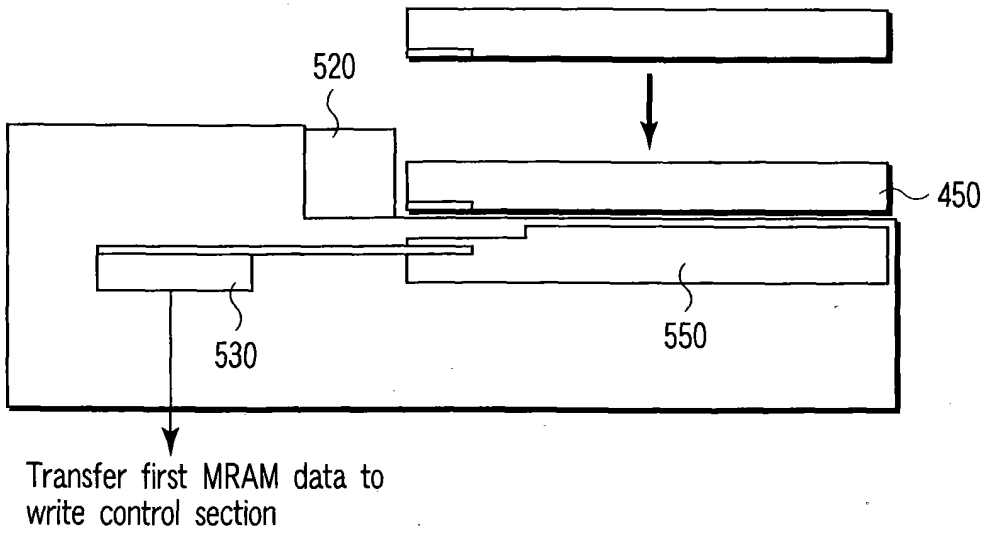

520
450
530
550
Transfer first MRAM data to
write control section

FIG. 26

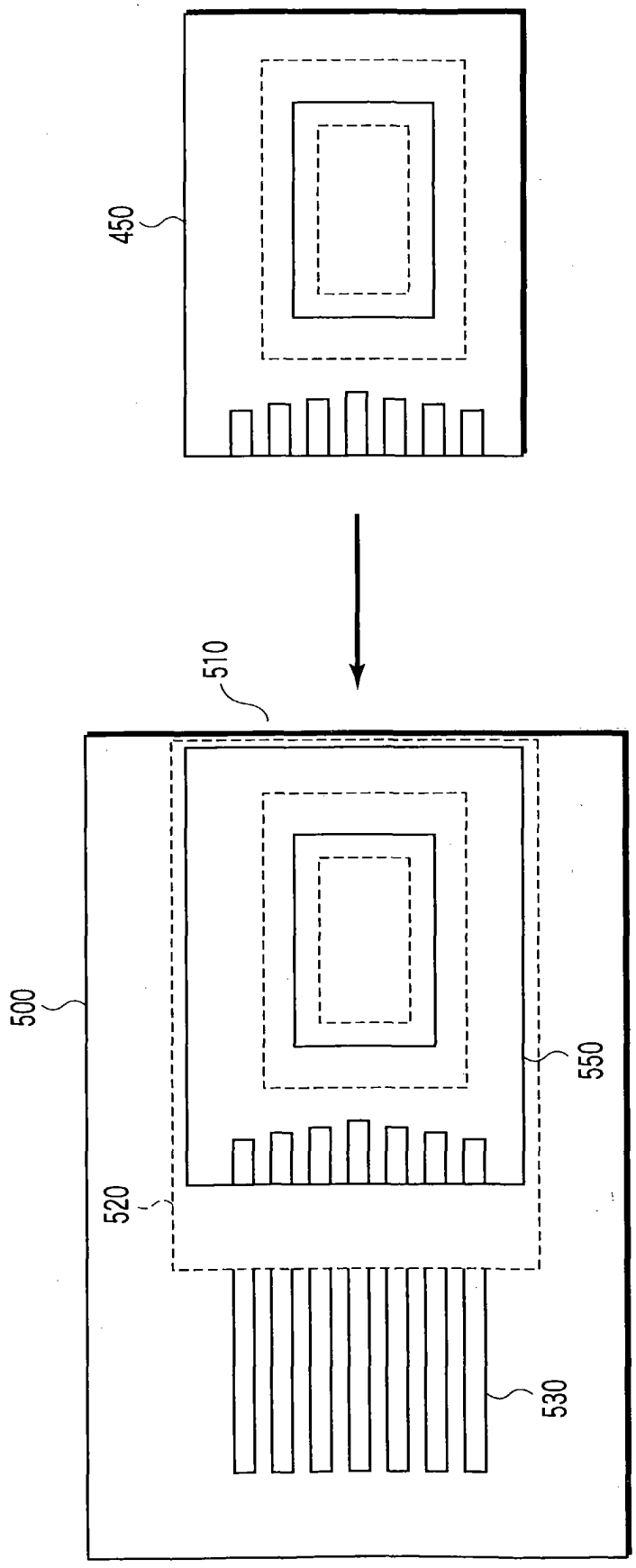


FIG. 24

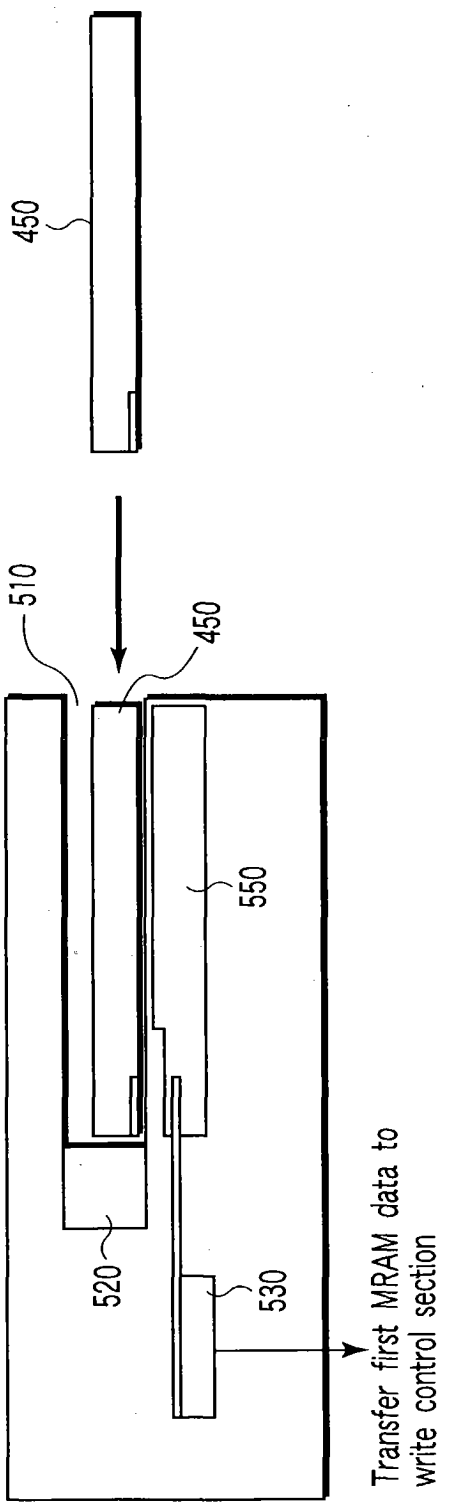

450
510
450
550
520
530
Transfer first MRAM data to write control section

FIG. 25

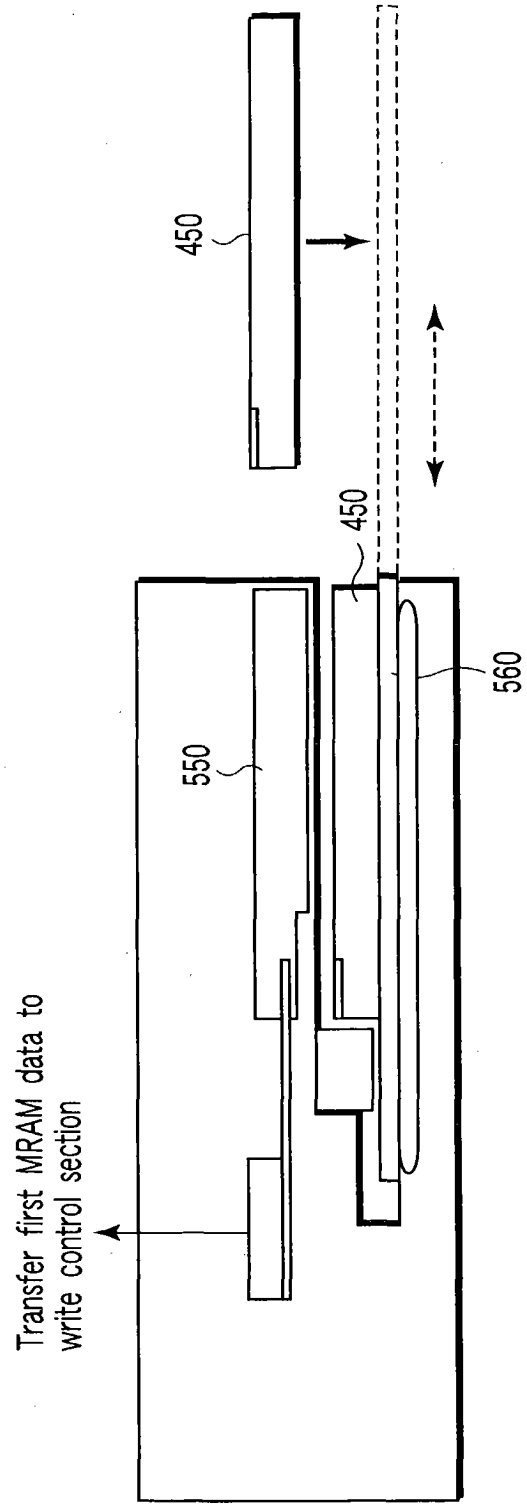

450
450
560
550
Transfer first MRAM data to write control section

FIG. 27